

Appl. No. 09/746,676

Attorney Docket: 042390.P10141

LISTING OF THE CLAIMS:

This listing of claims replaces all prior versions, and listings, of claims in the application:

- 1 1: (Currently Amended) An apparatus which comprises:
2 a multi-core processor and
3 at least one test control mechanism, including at least one test access port controller
4 (TAPC) and a plurality of distributed data and control registers;
5 **wherein said at least one test access port controller (TAPC) and at least one of said**
6 **plurality of distributed data and control registers are coupled via an Integrated Test Bus**
7 **(ITB)**
8 said multi-core processor and said test control mechanism having a configuration so as to
9 allow testing of said multi-core processor.
- 1 2: (original) The apparatus of claim 1, wherein said multi-core processor comprises at least two
2 processor cores and at least one circuit comprising non-processor core logic.
- 1 3: (original) The apparatus of claim 2, wherein said multi-core processor and said test control
2 mechanism having a configuration so as to allow testing of at least two processor cores of said
3 multi-core processor.
- 1 4: (Previously Presented) The apparatus of claim 2, wherein said plurality of distributed data and
2 control registers are located both within said at least two processor cores and within said at least
3 one circuit comprising non-core logic.

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1 5: (original) The apparatus of claim 4, wherein said at least one test control mechanism is
2 substantially compliant with the IEEE 1149.1 specification.

1 6: (original) The apparatus of claim 4, wherein said at least one test access port controller
2 (TAPC) is located within said at least two processor cores.

1 7: (Cancelled) .

1 8: (original) The apparatus of claim 4, wherein said distributed test control mechanism is
2 controllable, at least in part, by one of said at least one test access port controller (TAPC).

1 9: (Previously Presented) The apparatus of claim 8, wherein which one of said at least one test
2 access port controllers (TAPCs) controls said distributed test control mechanism is dynamically
3 selectable during operation.

1 10: (original) The apparatus of claim 2, wherein at least one of the said at least two processor
2 cores comprises one test access port (TAP) which includes one test access port controller
3 (TAPC), and a plurality of distributed data and control registers.

1 11: (original) The apparatus of claim 10, wherein said test control mechanism and said at least
2 two processor cores are coupled so as to provide multiple coupling arrangements, said multiple
3 coupling arrangements being dynamically selectable during operation.

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1 12: (original) The apparatus of claim 11, wherein said multiple coupling arrangements are
2 selected from a group consisting essentially of coupling said test access ports substantially in
3 series, coupling said test access ports substantially in parallel and coupling said test access ports
4 for substantially independent operation.

1 13: (original) The apparatus of claim 10, wherein said at least one test control mechanism is
2 arranged to allow at least one of said at least two processor cores' said one test access port (TAP)
3 to be externally visible from said multi-core processor.

1 14: (original) The apparatus of claim 13, wherein said at least one test control mechanism is
2 arranged to allow only one of said at least two processor cores' said one test access port (TAP) to
3 be externally visible from said multi-core processor.

1 15: (original) The apparatus of claim 13, wherein said at least one test control mechanism is
2 arranged to allow the selection of which at least one of said at least two processor cores' said one
3 test access port (TAP) is externally visible from said multi-core processor to occur dynamically.

1 16: (original) The apparatus of claim 10, wherein said at least one test control mechanism is
2 coupled to produce during operation an error signal if the output signals of said at least two
3 processor cores' said one test access port (TAP) are not substantially equivalent.

1 17: (original) The apparatus of claim 2, wherein said at least one test control mechanism, said at
2 least one processor core and said at least one circuit comprising non-processor core logic are

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3 further coupled so as to allow testing of said at least one circuit comprising non-processor core
4 logic.

1 18: (Currently Amended) A system which comprises:

2 a computing platform, including:

3 a memory to store instructions;

4 a multi-core processor to process instructions which includes:

5 a plurality of processor cores;

6 at least one circuit comprising non-processor core logic and

7 a test control mechanism, including at least one test access port controller

8 (TAPC) and a plurality of distributed data and control registers,

9 wherein said at least one test access port controller (TAPC) and at

10 least one of said a plurality of distributed data and control registers are coupled via an

11 Integrated Test Bus (ITB);

12 said multi-core processor and said test control mechanism having a configuration so as to

13 allow testing of said plurality of processor cores.

1 19: (Previously Presented) The system of claim 18, wherein said multi-core processor and said

2 test control mechanism are capable of allowing testing of said at least one circuit comprising

3 non-processor core logic.

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1 20: (Previously Presented) The system of claim 18, wherein said plurality of distributed data and
2 control registers are located both within said plurality of processor cores and within said at least
3 one circuit comprising non-core logic.

1 21: (original) The system of claim 20, wherein said at least one test control mechanism is
2 substantially compliant with the IEEE 1149.1 specification.

1 22: (original) The system of claim 20, wherein said at least one test access port controller
2 (TAPC) is located within said plurality of two processor cores.

1 23: (Cancelled) .

1 24: (original) The system of claim 20, wherein said distributed test control mechanism is
2 controlled, at least in part, by one of said at least one test access port controller (TAPC).

1 25: (Previously Presented) The system of claim 24, wherein which one of said at least one test
2 access port controllers (TAPCs) controls said distributed test control mechanism is be
3 dynamically selected during operation.

1 26: (original) The system of claim 18, wherein each of the said at least two processor cores
2 comprises one test access port (TAP) which includes one test access port controller (TAPC), and
3 a plurality of distributed data and control registers.

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1 27: (original) The system of claim 26, wherein said test control mechanism and said at least two
2 processor cores are coupled so as to provide multiple coupling arrangements, said multiple
3 coupling arrangements being dynamically selected during operation.

1 28: (original) The system of claim 27, wherein said multiple coupling configurations are
2 selected from a group consisting essentially of coupling said test access ports substantially in
3 series, coupling said test access ports substantially in parallel, and coupling said test access ports
4 for substantially independent operation.

1 29: (original) The system of claim 26, wherein said test control mechanism is coupled to
2 produce, during operation, a signal that indicates whether the output signals of said at least two
3 processor cores' said one test access port (TAP) are equivalent or substantially equivalent.

1 30-37: (Cancelled).